

JAPANESE

[JP,2003-303785,A]

---

CLAIMS DETAILED DESCRIPTION TECHNICAL FIELD PRIOR ART EFFECT OF THE INVENTION  
TECHNICAL PROBLEM DESCRIPTION OF DRAWINGS DRAWINGS

---

[Translation done.]

\* NOTICES \*

Japan Patent Office is not responsible for any damages caused by the use of this translation.

- 1.This document has been translated by computer. So the translation may not reflect the original precisely.
- 2.\*\*\*\* shows the word which can not be translated.
- 3.In the drawings, any words are not translated.

---

CLAIMS

---

[Claim(s)]

[Claim 1] The manufacture method of a semiconductor device of carrying out containing the aluminum thin film formation process which forms in the front face of the above-mentioned semiconductor substrate the thin film which contains aluminum so that the above-mentioned contact hole may fill, heating the above-mentioned semiconductor substrate after the substrate film formation process which is the manufacture method of the semiconductor device which forms the thin film containing aluminum as the contact hole formed on a semiconductor substrate fills, and forms the thin film which contains silicon in the internal surface of the above-mentioned contact hole, and the above-mentioned substrate film formation process as the feature.

[Claim 2] A manufacture method of a semiconductor device according to claim 1 that a ratio of the amount of silicon supplied to the above-mentioned semiconductor substrate at the above-mentioned substrate film formation process over the amount of aluminum supplied to the above-mentioned semiconductor substrate at the above-mentioned aluminum thin film formation process is characterized by being 0.1% or more and 1% or less in an atomic ratio.

[Claim 3] A manufacture method of a semiconductor device according to claim 1 or 2 characterized by the above-mentioned substrate film formation process including a process which forms a thin film of polish recon with chemical vapor deposition.

[Claim 4] A manufacture method of a semiconductor device according to claim 1 to 3 characterized by including a process in which the above-mentioned aluminum thin film formation process forms a thin film which contains aluminum by spatter.

[Claim 5] A manufacture method of a semiconductor device according to claim 1 to 4 characterized by the above-mentioned aluminum thin film formation process including a process which heats the above-mentioned semiconductor substrate at 300 degrees C thru/or 400 degrees C.

---

[Translation done.]

\* NOTICES \*

Japan Patent Office is not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. \*\*\*\* shows the word which can not be translated.
3. In the drawings, any words are not translated.

---

DETAILED DESCRIPTION

---

[Detailed Description of the Invention]

[0001]

[The technical field to which invention belongs] Especially this invention relates to the manufacture method of a semiconductor device including the process which forms the thin film which contains aluminum so that the detailed contact hole formed on semiconductor substrates, such as a silicon substrate, may be embedded about the manufacture method of semiconductor devices, such as MOS FET.

[0002]

[Description of the Prior Art] In the manufacturing process of a semiconductor device, the electrode thin film which consists of aluminum so that the contact hole of the shape of the detailed shape of a hole (hole) formed on the silicon substrate and a trench (slot) may be filled is formed. Such an electrode thin film forms the ejection electrode of the element (for example, transistor) formed on the silicon substrate. Such a thin film was formed by forming an aluminum thin film by the spatter, conventionally, so that an aluminum atom may be supplied on a silicon substrate and a contact hole may be filled.

[0003]

[Problem(s) to be Solved by the Invention] However, the width of face and the path of a contact hole are becoming small with detailed-izing of a circuit pattern in recent years (to for example, 0.6 micrometers or less). On the other hand, since the depth of a contact hole hardly changes even if a circuit pattern is made detailed, the ratio (aspect ratio) of the depth of a contact hole to the width of face or the path of a contact hole becomes large (1 or more [ for example, ]).

[0004] Such width of face or a path were not able to form the aluminum thin film which fills a contact hole by the above-mentioned method good in the narrow contact hole where an aspect ratio is large. Specifically, there was a problem that a void (opening) was formed in the portion corresponding to a contact hole within an aluminum thin film. In a spatter, this is because an aluminum thin film grows so that the opening of a contact hole may be plugged up, before the building envelope of the contact hole where width of face and a path are small and where an aspect ratio is large is thoroughly filled with an aluminum atom.

[0005] Moreover, at the process of the time of membrane formation, or after that, from an aluminum thin film, the aluminum atom was spread to the diffusion field on a silicon substrate etc. (aluminum spike), and there was also a problem that the pn junction of an element was destroyed. Then, the object of this invention is offering the manufacture method of the semiconductor device which can embed the thin film containing aluminum good in the contact hole where the width of face and the path which were formed on the semiconductor substrate are narrow, and an aspect ratio's is large.

[0006] Other objects of this invention are offering the manufacture method of the semiconductor device which an aluminum atom's cannot diffuse easily from the thin film containing the aluminum embedded in the contact hole.

[0007]

[The means for solving a technical problem and an effect of the invention] Invention according to claim 1 for solving the above-mentioned technical problem It is the manufacture method of the semiconductor device which forms the thin film (11) which contains aluminum so that the contact hole (4) formed on the semiconductor substrate (1) may be filled. The substrate film formation process which forms the thin film (15) which contains silicon in the internal surface of the above-mentioned contact hole, It is the manufacture method of the semiconductor device characterized by including the aluminum thin film formation process which forms in the front face of the above-mentioned semiconductor substrate the thin film (11 16) which contains aluminum so that the above-mentioned contact hole may be filled after the above-mentioned substrate film formation process, heating the above-mentioned semiconductor substrate.

[0008] In addition, the alphabetic character in a parenthesis shows the response component in the below-mentioned operation gestalt etc. In the following and this term, it is the same. According to this invention, in advance of formation of the thin film (henceforth an "aluminum thin film") containing aluminum, the thin film (substrate layer) containing silicon is formed in the front face of a semiconductor substrate including the inner surface of a contact hole. The aluminum atom which is the aluminum thin film formation process carried out succeedingly, for example, is supplied on a semiconductor substrate by physical vapor deposition cannot arrive at the interior of the contact hole on a semiconductor substrate (especially wall) easily. However, the aluminum atom which reached portions other than the contact hole of a semiconductor substrate front face is movable into a contact hole, being spread on a substrate film. For this reason, some thin films with which the aluminum atom was formed in the portion outside the contact hole of a semiconductor substrate by depositing move so that it may flow in in a contact hole in accordance with the inner surface of a contact hole.

[0009] Thereby, the inside of a contact hole is filled good and an aluminum thin film grows. Especially, width of face and a path have a contact hole as narrow as 0.6 micrometers or less, and when an aspect ratio is as high as one or more, such a manufacture method is effective. Etching etc. may remove the portion with an unnecessary aluminum thin film after that. Thus, the semiconductor layer (you may be the substrate itself.) and aluminum thin film which could form the aluminum thin film embedded good in the contact hole, for example, have been exposed to a contact hole inner surface are electrically connectable.

[0010] Moreover, in case an aluminum thin film grows, a silicon atom is spread from a substrate layer to an aluminum thin film. Therefore, an aluminum thin film becomes a thing containing silicon. For this reason, the aluminum atom in an aluminum thin film can prevent destruction of the pn junction which it was hard coming to spread to the semiconductor layer (what consists of silicon especially) exposed to a contact hole inner surface, and was formed in the way among the semiconductor layers concerned by this.

[0011] A semiconductor substrate may be a silicon substrate. Moreover, a contact hole may be formed into the film formed on the semiconductor substrate. Invention according to claim 2 is the manufacture method of a semiconductor device according to claim 1 that the ratio of the amount of silicon supplied to the above-mentioned semiconductor substrate at the above-mentioned substrate film formation process over the amount of aluminum supplied to the above-mentioned semiconductor substrate at the above-mentioned aluminum thin film formation process is characterized by being 0.1% or more and 1% or less in an atomic ratio.

[0012] Thereby, migration of the aluminum atom by above-mentioned diffusion arises effectively, and can embed an aluminum thin film good in a contact hole. Moreover, generating of the silicon nodule by superfluous silicon can also be prevented. Invention according to claim 3 is the manufacture method of the semiconductor device according to claim 1 or 2 characterized by the above-mentioned substrate film formation process including the process which forms the thin film (15) of polish recon with chemical vapor deposition.

[0013] With chemical vapor deposition, a polish recon film (substrate film) can be formed also in the interior of a contact hole (wall etc.) at homogeneity. Membrane formation of an aluminum thin film shall be based on the spatter according to claim 4 which is an example of physical vapor deposition like, for example. Invention according to claim 5 is the manufacture method of the semiconductor device according to claim 1 to 4 characterized by the above-mentioned aluminum thin film formation process including the process which heats the above-mentioned semiconductor substrate at 300 degrees C thru/or 400 degrees C.

[0014] In an aluminum thin film formation process, by heating a semiconductor substrate at 300 degrees C or more, diffusion of an above-mentioned aluminum atom and a silicon atom is produced suitably, and an aluminum thin film can be embedded good in a contact hole. Moreover, diffusion of the aluminum atom to a semiconductor substrate etc. can be lessened from the aluminum thin film embedded in the contact hole by making heating temperature of a semiconductor substrate into 400 degrees C or less.

[0015]

[Embodiment of the Invention] Below, the gestalt of operation of this invention is explained to details with reference to an accompanying drawing. Drawing 1 is the illustration-cross section showing the structure of MOS FET (Metal Oxide Semiconductor Field Effect Transistor) manufactured with the application of the manufacture method of this invention.

[0016] The epitaxial layer 2 of n-mold is formed in the surface section of a silicon substrate 1. On the epitaxial layer 2, the cascade screen 3 of two or more ridge configurations is mutually allotted to parallel. Between the adjoining cascade screens 3, it is a hole (hole) 4. The cascade screen 3 contains the p-layer 5 by which the laminating was carried out toward the upper part from the lower part (epitaxial layer 2 side), the n+ layer 6, and the silicon oxide layer 7. The polish recon layer 8 prolonged from the upper part of an epitaxial layer 2 is formed in the interior of each cascade screen 3. The polish recon layer 8 has penetrated the p-layer 5 and the n+ layer 6, and is in contact with the silicon oxide layer 7 in the upper part (an epitaxial layer 2 side is an opposite hand). The polish recon layer 8 is electric-conduction-ized by addition of an impurity, and in a direction (it is drawing 1 and is a direction vertical to space) parallel to the length direction of a cascade screen 3, it has exposed outside and it functions as a gate electrode of FET.

[0017] The oxide film 9 is formed in the perimeter of the polish recon layer 8 except for the portion which touches the silicon oxide layer 7. Between the p-layers 5 of the adjoining cascade screen 3, the p+ layer 10 with thickness thinner than the p-layer 5 is formed in the portion which touches an epitaxial layer 2. The aluminum electrode layer 11 which uses aluminum (aluminum) as a principal component so that a hole 4 may be filled is formed in the upper part of a cascade screen 3 and the p+ layer 10. The aluminum electrode layer 11 contains a little (0.3% [ as opposed to / For example, / aluminum ] in an atomic ratio) silicon. The aluminum electrode layer 11 functions as an ejection electrode of the n+ layer 6.

[0018] the ratio (aspect ratio) of depth D [ as opposed to / in MOS FET of the above structures, the width of face W1 of a hole 4 is 0.6 micrometers, and / the width of face W1 of a hole 4 ] -- D/W1 is large (1 or more [ for example, ]). The width of face W2 of the polish recon layer 8 is 0.6 micrometers, and width-of-face W3 of the portion which exists in one side of the polish recon layer 8 among cascade screens 3 is 0.45 micrometers. Therefore, the width of face W4 of the element unit of this MOS FET is 2.1 micrometers.

[0019] Drawing 2 is an illustration-cross section for explaining the formation process of the aluminum electrode layer 11. first, a p+ layer 10 and cascade screen 3 (silicon substrate 1) top -- CVD (chemical vacuum deposition) -- the polish recon film 15 is formed of law (drawing 2 (a)). The polish recon film 15 is formed in the side (wall of a hole 4) of a cascade screen 3, the upper surface of a cascade screen 3, etc. by uniform thickness on an epitaxial layer 2. Thickness of the polish recon film 15 can be made into 100A.

[0020] Next, to the silicon substrate 1 in which it carried out in this way, and the polish recon film 15 was formed, of a spatter, an aluminum atom accumulates and the aluminum thin film 16 is formed (drawing 2 (b) - (d)). Under the present circumstances, a silicon substrate 1 is heated. Since the aluminum atom supplied by the spatter on the silicon substrate 1 cannot arrive at the interior of a hole 4 easily, in early stages of membrane formation, an aluminum atom is mainly deposited on the exterior of a hole 4, and forms the aluminum thin film 16. Since an aluminum atom is diffused in the polish recon film 15, some aluminum thin films 16 formed outside the hole 4 are moved so that it may flow in in a hole 4 (drawing 2 (b)).

[0021] Moreover, the silicon atom which constitutes the polish recon film 15 is also diffused into the aluminum thin film 16. Such is carried out, the hole 4 is gradually filled with the aluminum thin film 16 (drawing 2 (c)), and a hole 4 is thoroughly filled with the aluminum thin film 16 at the time of membrane formation termination. After suspending supply of the aluminum atom to a silicon substrate 1, it is good also as continuing heating of the suitable time amount silicon substrate 1. As for the ratio of the amount of silicon to the amount of aluminum supplied to a silicon substrate 1 at the above process (drawing 2 (a) - (d)), it is desirable to consider as the inside of the solid-solution limit community of the silicon to the aluminum in the heating temperature of the silicon substrate 1 in the process which forms the polish recon film 15. The silicon atom which constitutes the polish recon layer 8 moves into the whole-quantity aluminum thin film 16, and the polish recon layer 8 stops in this case, existing after membrane formation termination of the aluminum thin film 16 between the aluminum thin film 16 (aluminum electrode layer 11), the p+ layer 10, and a cascade screen 3.

[0022] Thus, the good aluminum electrode layer 11 without a void (opening) is obtained (drawing 2 (d)). Especially, width of face and a path have a hole 4 as narrow as 0.6 micrometers or less, and when an aspect ratio is as high as one or more, such a manufacture method is effective. The aluminum electrode layer 11 uses aluminum as a principal component, and becomes a thing containing a little (0.3% [ as opposed to / For example, / aluminum ] in an atomic ratio) silicon. After the aluminum electrode layer 11 is formed, the garbage of the aluminum electrode layer 11 is removed by etching etc.

[0023] Even when the aluminum electrode layer 11 contains the silicon in a solid-solution limit community, and a silicon substrate 1 is heated and it becomes an elevated temperature in the time of the aluminum electrode layer 11 formation by the spatter, or other processes, it is hard to diffuse the aluminum atom which constitutes the aluminum electrode layer 11 to the p+ layer 10, a cascade screen 3, an epitaxial layer 2, etc. Therefore, an aluminum atom is spread in the epitaxial layer 2 which constitutes an element, the p-layer 5, and the n+ layer 6, and pn junction is not destroyed.

[0024] By the formation method of this aluminum electrode layer 11, before forming the aluminum electrode layer 11, it is not necessary to form a barrier metal layer. Although explanation of 1 operation gestalt of this invention is as above, this invention can also carry it out with other gestalten. For example, the manufacture method concerning this invention can be applied, also when filling various contact holes of semiconductor devices other than MOS FET and forming a thin film.

[0025] For example, with the above-mentioned operation gestalt, the aluminum electrode layer 11 is formed so that it may connect with the p-layer 5 (semiconductor layer) exposed to the hole 4 (contact hole) side electrically, but it may be formed so that it may connect with the semiconductor layer (the substrate itself is included.) exposed to a contact hole base electrically. In this case, only the insulating material may be exposed to the paries medialis orbitae of a contact hole. Moreover, the aluminum electrode layer 11 may be electrically connected to the conductor exposed in a contact hole.

[0026] Width of face or a path may not be restricted to a thing 0.6 micrometers or less, but the contact hole embedding a thin film (electrode wiring) may be a thing thing which has larger width of face or a larger path than 0.6 micrometers. Moreover, an aspect ratio may not be restricted to one or more things, but the aspect ratio of the contact hole embedding a thin film (electrode wiring) may be less than one thing. In addition, it is possible to perform modification various in the range of the matter indicated by the claim.

[0027]

[Example 1] The relation of the amount of silicon and cross-section condition in the aluminum electrode layer 11 formed by the above-mentioned method, the relation between the amount of silicon and contact resistance, and the relation between the amount of silicon and the surface state of the silicon substrate 1 after aluminum electrode layer 11 exfoliation were investigated. Heating temperature of the silicon substrate 1 at the time of a spatter was made into 370 degrees C. The ratio (henceforth a "Si/aluminum ratio") of the amount of silicon to the amount of aluminum in the aluminum electrode layer 11 could be 0.2%, 0.3%, 1.0%, 2.0%, and 6.0% (all are atomic ratios). Si / aluminum ratio was changed by changing the thickness of the polish recon film 15 formed by the CVD method. That is, a Si/aluminum ratio is almost equal to the ratio of the amount of silicon supplied to a silicon substrate 1 with the CVD method over the amount of aluminum supplied to a silicon substrate 1 by the spatter.

[0028] Moreover, Si / aluminum ratio also formed 0% of aluminum electrode layer 11 for the comparison. That is, the polish recon film 15 was not formed beforehand, but the aluminum electrode layer 11 was formed. The electron microscope investigated the cross-section condition of the aluminum electrode layer 11, and the surface state of the silicon substrate 1 after aluminum electrode layer 11 exfoliation. The assessment result of the cross-section condition of the aluminum electrode layer 11 and the surface state of the silicon substrate 1 after aluminum electrode layer 11 exfoliation is shown in a table 1. The void etc. did not exist in the interior but the cross-section condition had [ 0.2 - 6.0% of aluminum electrode layer 11 ] all good Si / aluminum ratio. On the other hand, the void existed [ Si / aluminum ratio ] in 0% of aluminum electrode layer 11.

[0029] When Si/aluminum ratios were 0.0% and 0.2%, the trace of the aluminum spike to a silicon substrate 1

from the aluminum electrode layer 11 existed in the front face of the silicon substrate 1 after aluminum electrode layer 11 exfoliation. When Si/aluminum ratios were 2.0% and 6.0%, the nodule of silicon existed. When Si/aluminum ratios were 0.3% and 1.0%, neither the trace of an aluminum spike nor the nodule of silicon existed, but was good.

[0030] From the above thing, a Si/aluminum ratio is understood that 0.2% thru/or 1.0% are desirable. Since an aluminum spike occurs when a Si/aluminum ratio is 0.2%, a Si/aluminum ratio can be made into 0.3% thru/or 1.0% still more preferably. The above is a result in case the heating temperature of a silicon substrate 1 is 370 degrees C, and when the heating temperature of a silicon substrate 1 differs, it is expected that the ranges of the optimal Si/aluminum ratio differ.

[0031]

[A table 1]

|               | 比較例    | 実施例    | 実施例 | 実施例 | 実施例     | 実施例     |
|---------------|--------|--------|-----|-----|---------|---------|
| Si/Al (atom%) | 0.0    | 0.2    | 0.3 | 1.0 | 2.0     | 6.0     |
| 電極膜断面のポイド     | あり     | なし     | なし  | なし  | なし      | なし      |
| 剥離後表面状態       | スパイクあり | スパイクあり | 良好  | 良好  | ノジュールあり | ノジュールあり |

[0032] Drawing 3 is drawing showing the relation between Si / aluminum ratio, and contact resistance. contact resistance shows the low value of about 1 law below by 0.5microomega, when a Si/aluminum ratio is 0 - 0.3%, but when a Si/aluminum ratio is 1.0% or more, it becomes large with the increment in a Si/aluminum ratio. When a Si/aluminum ratio is 2.0% or more, contact resistance becomes about 5.0-5.5microhm.

[0033]

[Example 2] The relation between the heating temperature of the silicon substrate 1 at the time of aluminum electrode layer 11 formation, and the cross-section condition of the aluminum electrode layer 11 and the obtained FET On resistance of a semiconductor device was investigated. The Si/aluminum ratio could be 0.3%. Heating temperature of a silicon substrate 1 was made into 275 degrees C, 340 degrees C, 410 degrees C, 480 degrees C, and 550 degrees C. The assessment result of the cross-section condition of the aluminum electrode layer 11 is shown in a table 2. The void etc. did not exist but the condition of a cross section of the aluminum electrode layer 11 in which the heating temperature of a silicon substrate 1 was formed at 340-480 degrees C was all good. On the other hand, the void existed in the aluminum electrode layer 11 in which the heating temperature of a silicon substrate 1 was formed at 275 degrees C.

[0034]

[A table 2]

| スパッタ加熱温度(°C) | 275 | 340 | 410 | 480 |
|--------------|-----|-----|-----|-----|
| 電極膜断面のポイド    | あり  | なし  | なし  | なし  |

[0035] Drawing 4 is drawing showing the relation between the heating temperature of a silicon substrate 1, and FET On resistance. FET On resistance shows about 80m ohm and a low value, when the heating temperature of a silicon substrate 1 is 275-410 degrees C, but when the heating temperature of a silicon substrate 1 is 550 degrees C, it becomes high with about 160mohm. From the above thing, the heating temperature of a silicon substrate 1 is understood that 300-400 degrees C is desirable.

[Translation done.]

\* NOTICES \*

Japan Patent Office is not responsible for any damages caused by the use of this translation.

- 1.This document has been translated by computer. So the translation may not reflect the original precisely.
- 2.\*\*\*\* shows the word which can not be translated.
- 3.In the drawings, any words are not translated.

---

DESCRIPTION OF DRAWINGS

---

[Brief Description of the Drawings]

[Drawing 1] It is the illustration-cross section showing the structure of MOS FET manufactured with the application of the manufacture method of this invention.

[Drawing 2] It is an illustration-cross section for explaining the formation method of an aluminum electrode.

[Drawing 3] It is drawing showing the relation of the ratio of the amount of silicon and contact resistance to the amount of aluminum in an aluminum electrode.

[Drawing 4] It is drawing showing the relation between the heating temperature of a silicon substrate, and FET On resistance.

[Description of Notations]

1 Silicon Substrate

4 Hole

11 Aluminum Electrode Layer

15 Polish Recon Film

16 Aluminum Thin Film

---

[Translation done.]